

Document Title

1M x 32 Bit x 4 Banks (128-MBIT) DDR SDRAM

Revision History

<u>Revision No</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0A	Initial Draft	July 21,2004	
0B	Mass production	November 10,2004	

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1M Words x 32 Bits x 4 Banks (128-MBIT)

DDR SYNCHRONOUS DYNAMIC RAM

FEATURES

- Fast clock rate: 250/200 MHz
- Differential Clock CK & CK# input
- 4 Bi-directional DQS. Data transactions on both edges of DQS (1DQS / Byte)
- DLL aligns DQ and DQS transitions
- Edge aligned data & DQS output
- Center aligned data & DQS input
- 4 internal banks, 1M x 32-bit for each bank
- Programmable mode and extended mode registers
 - CAS# Latency: 3, 4, 5
 - Burst length: 2, 4, 8
 - Burst Type: Sequential & Interleave
- Full page burst length for sequential type only
- Start address of full page burst should be even
- All inputs except DQ's & DM are at the positive edge of the system clock
- No Write-Interrupted by Read function
- 4 individual DM control for write masking only
- Auto Refresh and Self Refresh
- 4096 refresh cycles / 32ms
- Power supplies up to 250/200MHz:
 - VDD = 2.5V +/- 5%
 - VDDQ = 2.5V +/- 5%
- Interface : SSTL_2 I/O compatible
- Standard 144-ball FBGA package
- Support Green Package

Overview

The IC43R32400 DDR SDRAM is a high-speed CMOS double data rate synchronous DRAM containing 128 Mbits. It is internally configured as a quad 1M x 32 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CK).

Data outputs occur at both rising edges of CK and CK#. Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

Accesses begin with the registration of a BankActivate command, which is then followed by a Read or Write command.

The IC43R32400 provides programmable Read or Write burst lengths of 2, 4, 8. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

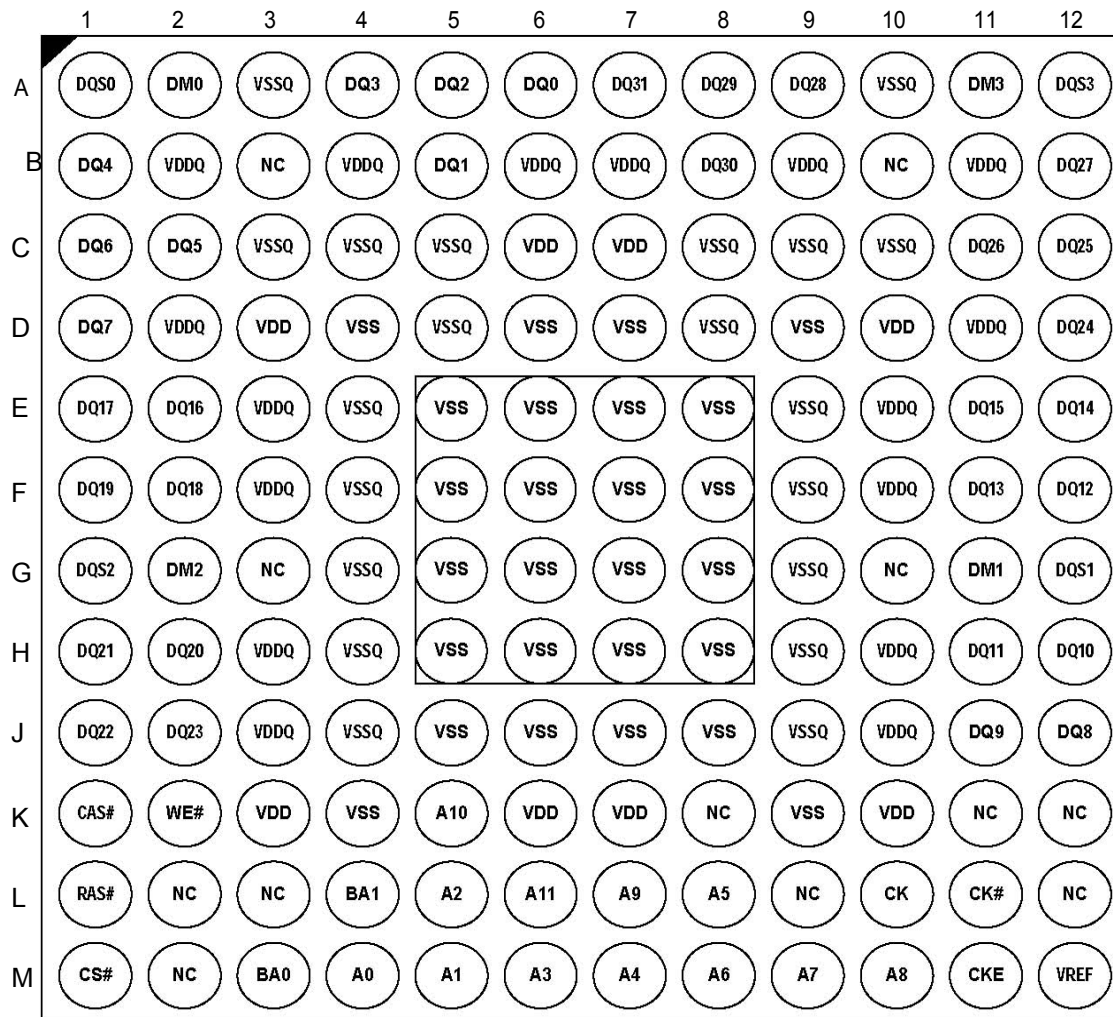
The refresh functions, either Auto or Self Refresh are easy to use.

In addition, IC43R32400 features programmable DLL option. By having a programmable mode register and extended mode register, the system can choose the most suitable modes to maximize its performance.

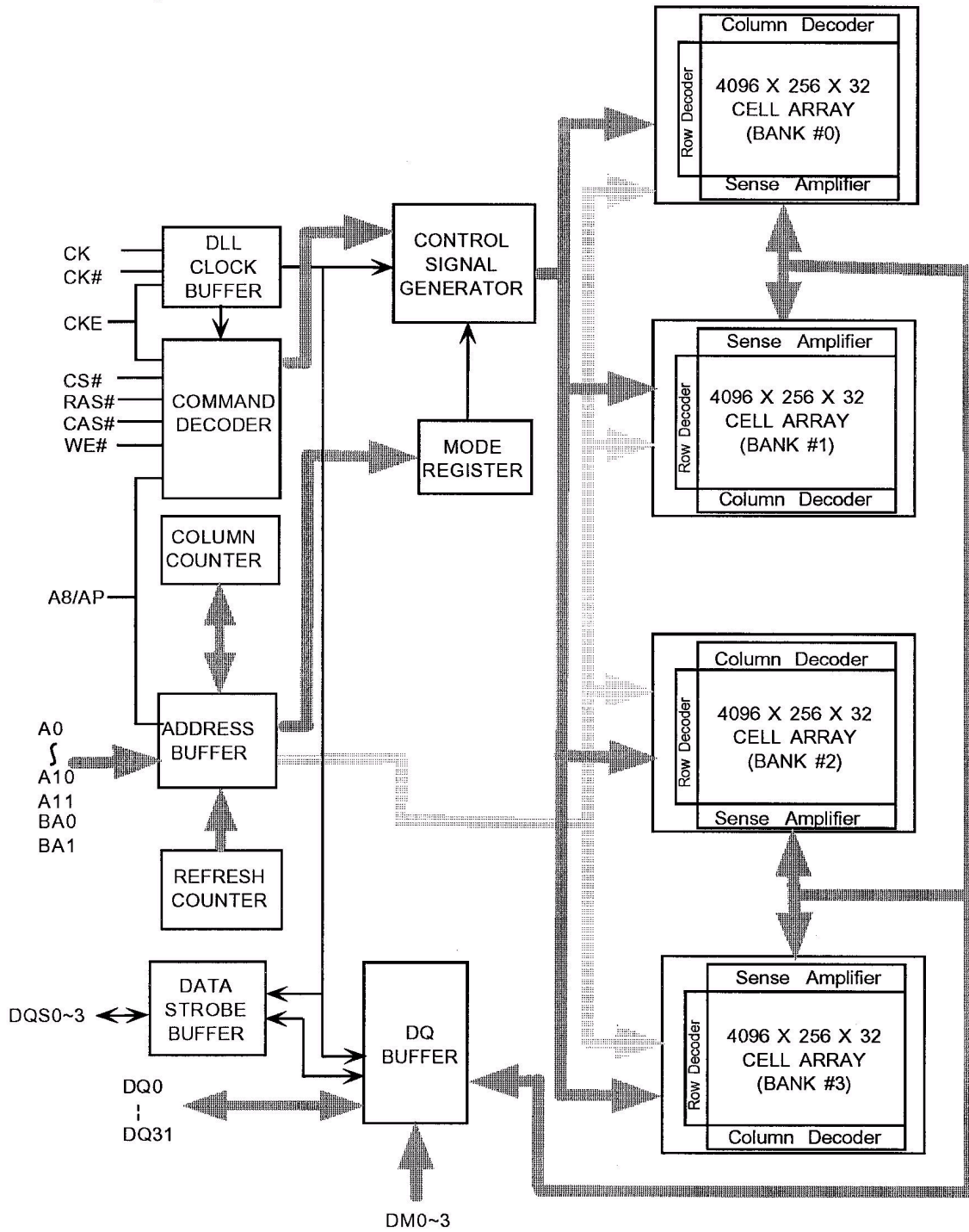
These devices are well suited for applications requiring high memory bandwidth, result in a device particularly well suited to high performance main memory and graphics applications.

IC43R32400

Pin Assignment (FBGA 144Ball Top View) Note: VSS pins for thermal balls are optional



Block Diagram



IC43R32400

PIN DESCRIPTIONS

Table 1.Pin Details of IC43R32400

Symbol	Type	Description
CK,CK#	Input	Differential Clock: CK, CK# are driven by the system clock. All SDRAM input commands are sampled on the positive edge of CK. Both CK and CK# increment the internal burst counter and controls the output registers.
CKE	Input	Clock Enable: CKE activates(HIGH)and deactivates(LOW)the CK signal.If CKE goes low synchronously with clock,the internal clock is suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low.When all banks are in the idle state, deactivating the clock controls the entry to the Power Down and Self Refresh modes.
BS0,BS1	Input	Bank Select: BA0 and BA1 defines to which bank the BankActivate,Read,Write,or BankPrecharge command is being applied. They also define which Mode Register or Extended Mode Register is loaded during a Mode Register Set command.
A0-A11	Input	Address Inputs: A0-A10 are sampled during the BankActivate command (row address A0-A11) and Read/Write command (column address A0-A7 with A8 defining Auto Precharge) to select one location out of the 256K available in the respective bank.During a Precharge command,A8 is sampled to determine if all banks are to be precharged (A8 =HIGH).The address inputs also provide the op-code during a Mode Register Set or Extended Mode Register Set command.
CS#	Input	Chip Select: CS# enables (sampled LOW)and disables (sampled HIGH)the command decoder.All commands are masked when CS#is sampled HIGH.CS#provides for external bank selection on systems with multiple banks.It is considered part of the command code.
RAS#	Input	Row Address Strobe: The RAS# signal defines the operation commands in conjunction with the CAS# and WE# signals and is latched at the positive edges of CK.When RAS# and CS# are asserted "LOW"and CAS# is asserted "HIGH,"either the BankActivate command or the Precharge command is selected by the WE# signal.When the WE# is asserted "HIGH,"the BankActivate command is selected and the bank designated by BS is turned on to the active state.When the WE# is asserted "LOW,"the Precharge command is selected and the bank designated by BS is switched to the idle state after the precharge operation.
CAS#	Input	Column Address Strobe: The CAS# signal defines the operation commands in conjunction with the RAS# and WE# signals and is latched at the positive edges of CK. When RAS# is held "HIGH"and CS# is asserted "LOW,"the column access is started by asserting CAS# "LOW."Then, the Read or Write command is selected by asserting WE# "HIGH"or "LOW."
WE#	Input	Write Enable: The WE# signal defines the operation commands in conjunction with the RAS# and CAS# signals and is latched at the positive edges of CK.The WE# input is used to select the BankActivate or Precharge command and Read or Write command.
DQS0-DQS3	Input/Output	Bidirectional Data Strobe: The DQSx signals are mapped to the following data bytes: DQS0 to DQ0-DQ7, DQS1 to DQ8-DQ15, DQS2 to DQ16-DQ23, DQS3 to DQ24-DQ31.
DM0-DM3	Input	Data Input Mask: DM0-DM3 are byte specific. Input data is masked when DM is sampled HIGH during a write cycle. DM3 masks DQ31-DQ24, DM2 masks DQ23DQ16, DM1 masks DQ15-DQ8, and DM0 masks DQ7-DQ0.
DQ0-DQ31	Input/Output	Data I/O: The DQ0-DQ31 input and output data are synchronized with the positive edges of CK and CK#.The I/Os are byte-maskable during Writes.
V _{DD}	Supply	Power Supply: Power for the input buffers and core logic.

V _{SS}	Supply	Ground: Ground for the input buffers and core logic.
V _{DDQ}	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
V _{SSQ}	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
V _{REF}	Supply	Reference Voltage for Inputs: +0.5 x V _{DDQ}
NC	-	No Connect: These pins should be left unconnected.

Note: The timing reference point for the differential clocking is the cross point of the CK and CK#. For any applications using the single ended clocking, apply V_{REF} to CK# pin.

Operation Mode

Fully synchronous operations are performed to latch the commands at the positive edges of CK. Table 2 shows the truth table for the operation commands.

Table 2. Truth Table (Note (1), (2))

Command	State	CKEn-1	CKEn	DM	BA1	BA0	A8	A11-A9,A7-0	CS#	RAS#	CAS#	WE#
BankActivate	Idle ⁽³⁾	H	X	X	V	V	Row address		L	L	H	H
BankPrecharge	Any	H	X	X	V	V	L	X	L	L	H	L
PrechargeAll	Any	H	X	X	X	X	H	X	L	L	H	L
Write	Active ⁽³⁾	H	X	V	V	V	L	Column address	L	H	L	L
Write and Auto Precharge	Active ⁽³⁾	H	X	V	V	V	H		L	H	L	L
								A0~A7				
Read	Active ⁽³⁾	H	X	X	V	V	L	Column address	L	H	L	H
Read and Autoprecharge	Active ⁽³⁾	H	X	X	V	V	H		L	H	L	H
								A0~A7				
Mode Register Set	Idle	H	X	X	L	L	OP code		L	L	L	L
Extended Mode Register Set	Idle	H	X	X	L	H	OP code		L	L	L	L
No-Operation	Any	H	X	X	X	X	X	X	L	H	H	H
Device Deselect	Any	H	X	X	X	X	X	X	H	X	X	X
Burst Stop	Any ⁽⁴⁾	H	X	X	X	X	X	X	L	H	H	L
AutoRefresh	Idle	H	H	X	X	X	X	X	L	L	L	H
SelfRefresh Entry	Idle	H	L	X	X	X	X	X	L	L	L	H
SelfRefresh Exit	Idle	L	H	X	X	X	X	X	H	X	X	X
	(SelfRefresh)								L	H	H	H
Power Down Mode Entry	Idle/Active ⁽⁵⁾	H	L	X	X	X	X	X	H	X	X	X
									L	H	H	H
Power Down Mode Exit	Any	L	H	X	X	X	X	X	H	X	X	X
	(PowerDown)								L	H	H	H
Data Write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X	X
Data Mask/Output Disable	Active	H	X	H	X	X	X	X	X	X	X	X

Note:

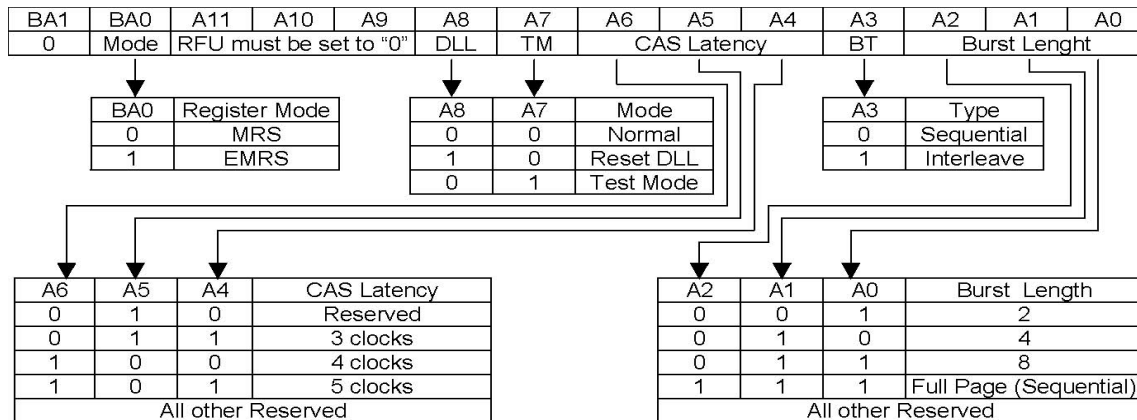
1. V =Valid Data, X =Don't care, L =Low level, H = High level
2. CKEn signal is input level when commands are provided.
CKEn-1 signal is input level one clock cycle before the commands are provided.
3. These are states of bank designated by BA1 signals.
4. Read burst stop with BST command for all burst types.
5. Power Down Mode can not enter in the burst operation.
When this command is asserted in the burst cycle,device state is clock suspend mode.

Mode Register Set (MRS)

The mode register is divided into various fields depending on functionality.

- **Burst Length Field (A2, A1, A0)**
This field specifies the data length of column access and selects the Burst Length.
- **Addressing Mode Select Field (A3)**
The Addressing Mode can be Interleave Mode or Sequential Mode. Both Sequential Mode and Interleave Mode support burst length of 2, 4 and 8. Full page burst length is only for Sequential mode.
- **CAS# Latency Field (A6, A5, A4)**
This field specifies the number of clock cycles from the assertion of the Read command to the first read data. The minimum whole value of CAS# Latency depends on the frequency of CK. The minimum whole value satisfying the following formula must be programmed into this field.
 $t_{CAC(min)} _ CAS\# \text{ Latency} \times t_{CK}$
- **Test Mode field :A7; DLL Reset Mode field : A8**
These two bits must be programmed to "00" in normal operation.
- (BA0, BA1)

Mode Resistor Bitmap



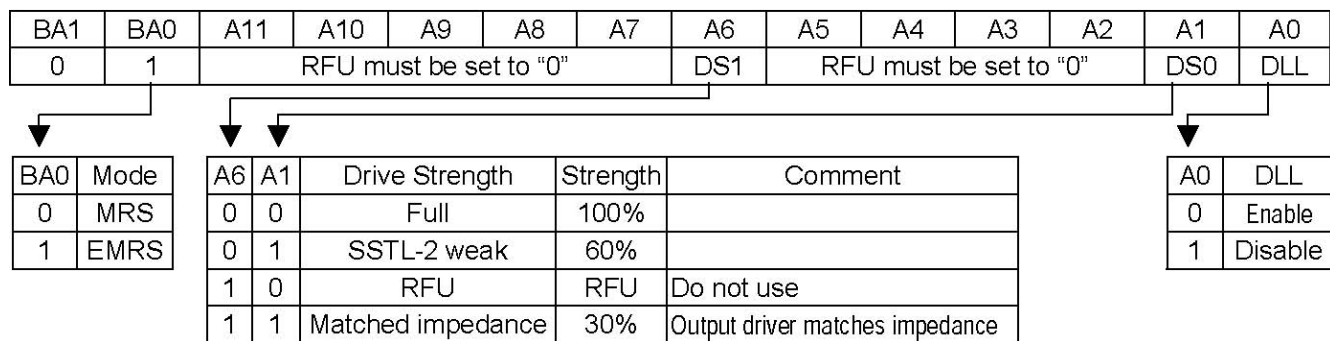
Brst Definition, Addressing Sequence of Sequential and Interleave Mode

Burst Length	Start Address			Sequential	Interleave
	A2	A1	A0		
2	X	X	0	0, 1	0, 1
	X	X	1	1, 0	1, 0
4	X	0	0	0, 1, 2, 3	0, 1, 2, 3
	X	0	1	1, 2, 3, 0	1, 0, 3, 2
	X	1	0	2, 3, 0, 1	2, 3, 0, 1
	X	1	1	3, 0, 1, 2	3, 2, 1, 0
8	0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0	0	1	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	0	1	0	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	0	1	1	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1	0	1	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	1	1	0	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	1	1	1	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Extended Mode Register Set (EMRS)

The Extended Mode Register Set stores the data for enabling or disabling DLL and selecting output driver strength. The default value of the extended mode register is not defined, therefore must be written after power up for proper operation. The extended mode register is written by asserting low on CS#, RAS#, CAS#, and WE#. The state of A0, A2 ~ A5, A7 ~ A11 and BA1 is written in the mode register in the same cycle as CS#, RAS#, CAS#, and WE# going low. The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register. A1 and A6 are used for setting driver strength to normal, weak or matched impedance. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. "High" on BA0 is used for EMRS. Refer to the table for specific codes.

Extended Mode Resistor Bitmap



Power up Sequence

Power up must be performed in the following sequence.

- 1) Apply power to VDD before or at the same time as VDDQ, VTT and VREF when all input signals are held "NOP" state and maintain CKE "LOW".
- 2) Start clock and maintain stable condition for minimum 200us.
- 3) Issue a "NOP" command and keep CKE "HIGH"
- 4) Issue a "Precharge All" command.
- 5) Issue EMRS – enable DLL.
- 6) Issue MRS – reset DLL. (An additional 200 clock cycles are required to lock the DLL).
- 7) Precharge all banks of the device.
- 8) Issue two or more Auto Refresh commands.
- 9) Issue MRS – with A8 to low to initialize the mode register.

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Absolute Maximum Rating

Symbol	Item	Rating	Unit	Note
V _{IN} ,V _{OUT}	Input,Output Voltage	-0.3~V _{DDQ} +0.3	V	
V _{DD} ,V _{DDQ}	Power Supply Voltage	-0.3~3.6	V	
T _A	Ambient Temperature	0~70	°C	
T _{STG}	Storage Temperature	-55~150	°C	
T _{SOLDER}	Soldering Temperature (10s)	260	°C	
P _D	Power Dissipation	2.0	W	
I _{OUT}	Short Circuit Output Current	50	mA	

Recommended D.C.Operating Conditions (SSTL_2 In/Out, Ta =0~70+/- °C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Note
V _{DD}	Power Supply Voltage	2.375	2.5	2.625	V	
V _{DDQ}	Power Supply Voltage(for I/O)	2.375	2.5	2.625	V	
V _{REF}	Input Reference Voltage	0.49x V _{DDQ}	-	0.51x V _{DDQ}	V	
V _{TT}	Termination Voltage	V _{REF} - 0.04	V _{REF}	V _{REF} + 0.04	V	
V _{IH(DC)}	Input High Voltage	V _{REF} + 0.15	-	V _{DDQ} +0.3	V	
V _{IL(DC)}	Input Low Voltage	V _{ssq} - 0.3	-	V _{DDQ} -0.15	V	
V _{OH}	Output High Voltage	V _{tt} + 0.76	-	-	V	I _{OH} = -15.2 mA
V _{OL}	Output Low Voltage	-	-	V _{REF} - 0.76	V	I _{OL} = +15.2 mA
I _{IL}	Input Leakage Current	- 5	-	5	uA	
I _{OL}	Output Leakage Current	- 5	-	5	uA	

Note: Under all conditions V_{DDQ} must bbe less than or equal to V_{DD}.

Capacitance (VDD =2.5V, f =1MHz,Ta =25+/- °C)

Symbol	Parameter	Min.	Max.	Unit
C _{IN1}	Input Capacitance (A0~A11, BA0, BA1)	4	5	pF
C _{IN2}	Input Capacitance(CK, CK#,CKE, CS#,RAS#, CAS #,WE#)	3	5	pF
C _{OUT}	DQ & DQS input/output capacitance	6	8	pF
C _{IN3}	DM0~DM3 input/output capacitance	6	8	pF

Note: These parameters are periodically sampled and are not 100% tested.

D.C. Characteristics

(VDD = 2.5V +/- 5%, TA = 0~70 °C)

Parameter & Test Condition	Symbol	4	5	Unit
		Max		
OPERATING CURRENT : One bank; Active-Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles.	IDD0	180	160	mA
OPERATING CURRENT : One bank; Active-Read-Precharge; BL=4; CL=4; tRCDRD=4*tCK; tRC=tRC(min); tCK=tCK(min); Iout=0mA; Address and control inputs changing once per clock cycle	IDD1	260	240	mA
PRECHARGE POWER-DOWN STANDBY CURRENT : All banks idle; power-down mode; tCK=tCK(min); CKE=LOW	IDD2P	45	40	mA
IDLE STANDBY CURRENT : CKE = HIGH; CS#=HIGH(DESELECT); All banks idle; tCK=tCK(min); Address and control inputs changing once per clock cycle; VIN=VREF for DQ, DQS and DM	IDD2N	80	80	mA
ACTIVE POWER-DOWN STANDBY CURRENT : one bank active; power-down mode; CKE=LOW; tCK=tCK(min)	IDD3P	45	40	mA
ACTIVE STANDBY CURRENT : CS#=HIGH; CKE=HIGH; one bank active ; tRC=tRC(max);tCK=tCK(min);Address and control inputs changing once per clock cycle; DQ,DQS,and DM inputs changing twice per clock cycle	IDD3N	100	100	mA
OPERATING CURRENT BURST READ : BL=2; READS; Continuous burst; one bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); Iout=0mA;50% of data changing on every transfer	IDD4R	440	420	mA
OPERATING CURRENT BURST Write : BL=2; WRITES; Continuous Burst ;one bank active; address and control inputs changing once per clock cycle; tCK=tCK(min); DQ,DQS,and DM changing twice per clock cycle; 50% of data changing on every transfer	IDD4W	300	270	mA
AUTO REFRESH CURRENT : tRC=tRFC(min); tCK=tCK(min)	DD5	300	280	mA
SELF REFRESH CURRENT : Self Refresh Mode ; CKE<=0.2V;tCK=tCK(min)	IDD6	3	3	mA
BURST OPERATING CURRENT 4 bank operation : Four bank interleaving READs; BL=4;with Auto Precharge; tRC=tRC(min); tCK=tCK(min); Address and control inputschang only during Active, READ , or WRITE command	IDD7	650	550	mA

- Note:** 1.Stress greater than those listed under " Absolute maximum Ratings" may cause permanent damage of the device.
 2.All voltages are referenced to Vss.
 3.Power-up sequence is described in previous page.

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Decoupling Capacitance Guide Line

Symbol	Parameter	Value	Unit
C _{DC1}	Decoupling Capacitance between V _{DD} and V _{SS}	0.1+0.01	uF
C _{DC2}	Decoupling Capacitance between V _{DDQ} and V _{SSQ}	0.1+0.01	uF

AC Input Operating Conditions

(V_{DD} = 2.5V +/- 5%, T_a = 0~70 °C)

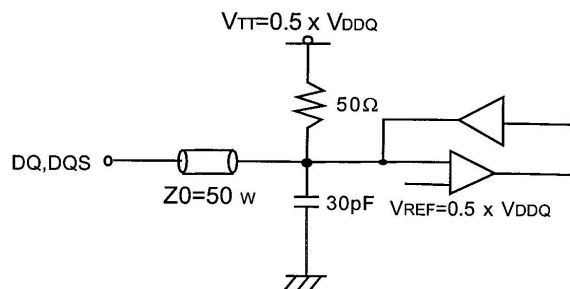
Symbol	Parameter	Min	Max	Unit
V _{IH}	Input High Voltage; DQ	V _{REF} +0.4	-	V
V _{IL}	Input Low Voltage; DQ	-	V _{REF} -0.4	V
V _{ID}	Clock Input Differential Voltage; Ck & CK#	0.8	V _{DDQ} +0.6	V
V _{IX}	Clock Input Crossing Point Voltage; Ck & CK#	0.5xV _{DDQ} -0.2	0.5xV _{DDQ} +0.2	V

AC Operating Test Conditions

(V_{DD} = 2.5V +/- 5%, T_a = 0~70 °C)

Reference Level of Output Signals (V _{RFE})	0.5 x V _{DDQ}
CK & CK# signal maximum peak swing	1.5V
Output Load	See Figure. A Test Load
Input Signal Levels	V _{REF} +0.4 V / V _{REF} -0.4 V
Input Signals Slew Rate	1 V/ns
Input timing measurement reference level	V _{REF}
Output timing measurement reference level	V _{TT}
Reference Level of Input Signals	0.5 x V _{DDQ}

Figure A. Test Load



Electrical Characteristics and Recommended A.C. Operating Conditions

(VDD = 2.5V +/- 5%, Ta = 0~70 °C)

Symbol	Parameter	4.0		5.0		Unit	
		Min	Man	Min	Max		
tCK	Clock cycle time	CL = 3	4	10	5	10	ns
		CL = 4	4	10	5	10	
		CL = 5	4	5	5	10	
tCH	Clock high level width	0.45	0.55	0.45	0.55	tCK	
tCL	Clock low level width	0.45	0.55	0.45	0.55	tCK	
tDQCK	DQS-out access time from CK,CK#	-0.7	0.7	-0.7	0.7	ns	
tAC	Output access time from CK,CK#	-0.7	0.7	-0.7	0.7	ns	
tDQSQ	DQS-DQ Skew	-	0.4	-	0.45	ns	
tRPRE	Read preamble	0.9	1.1	0.9	1.1	tCK	
tRPST	Read postamble	0.4	0.6	0.4	0.6	tCK	
tDQSS	CK to valid DQS-in	0.85	1.15	0.85	1.15	tCK	
tWPRES	DQS-in setup time	0	-	0	-	ns	
tWPREH	DQS-in hold time	0.35	-	0.35	-	ns	
tWPST	DQS write postamble	0.4	0.6	0.4	0.6	tCK	
tDQSH	DQS in high level pulse width	0.4	0.6	0.4	0.6	tCK	
tDQSL	DQS in low level pulse width	0.4	0.6	0.4	0.6	tCK	
tIS	Address and Control input setup time	0.9	-	1.0	-	ns	
tDS	DQ & DM setup time to DQS	0.45	-	0.5	-	ns	
tDH	DQ & DM hold time to DQS	0.45	-	0.5	-	ns	
tHP	Clock half period	tCLMIN or tCHMIN	-	tCLMIN or tCHMIN	-	ns	
tQH	Output DQS valid window	tHP- 0.45	-	tHP - 0.5	-	ns	
tRC	Row cycle time	15	-	12	-	tCK	
tRFC	Refresh row cycle time	17	-	14	-	tCK	
tRAS	Row active time	10	100K	8	100K	tCK	
tRCDRD	RAS# to CAS# Delay in Read	5	-	4	-	tCK	
tRCDWR	RAS# to CAS# Delay in Write	3	-	2	-	tCK	
tRP	Row precharge time	3	-	3	-	tCK	
tRRD	Row active to Row active delay	3	-	2	-	tCK	
tWR	Write recovery time	3	-	2	-	tCK	
tCDLR	Last data in to Read command	2	-	2	-	tCK	
tCCD	Col. Address to Col. Address delay	1	-	1	-	tCK	
tMRD	Mode register set cycle time	2	-	2	-	tCK	
tDAL	Auto precharge write recovery + Precharge	8	-	7	-	tCK	
tXSA	Self refresh exit to read command delay	200	-	200	-	tCK	
tPDEX	Power down exit time	tIS + 2tCK	-	tIS + 2tCK	-	ns	
tREF	Refresh interval time	-	7.8	-	7.8	us	

Timing Waveforms

Figure 1. AC Parameters for Read Timing (Burst Length =4)

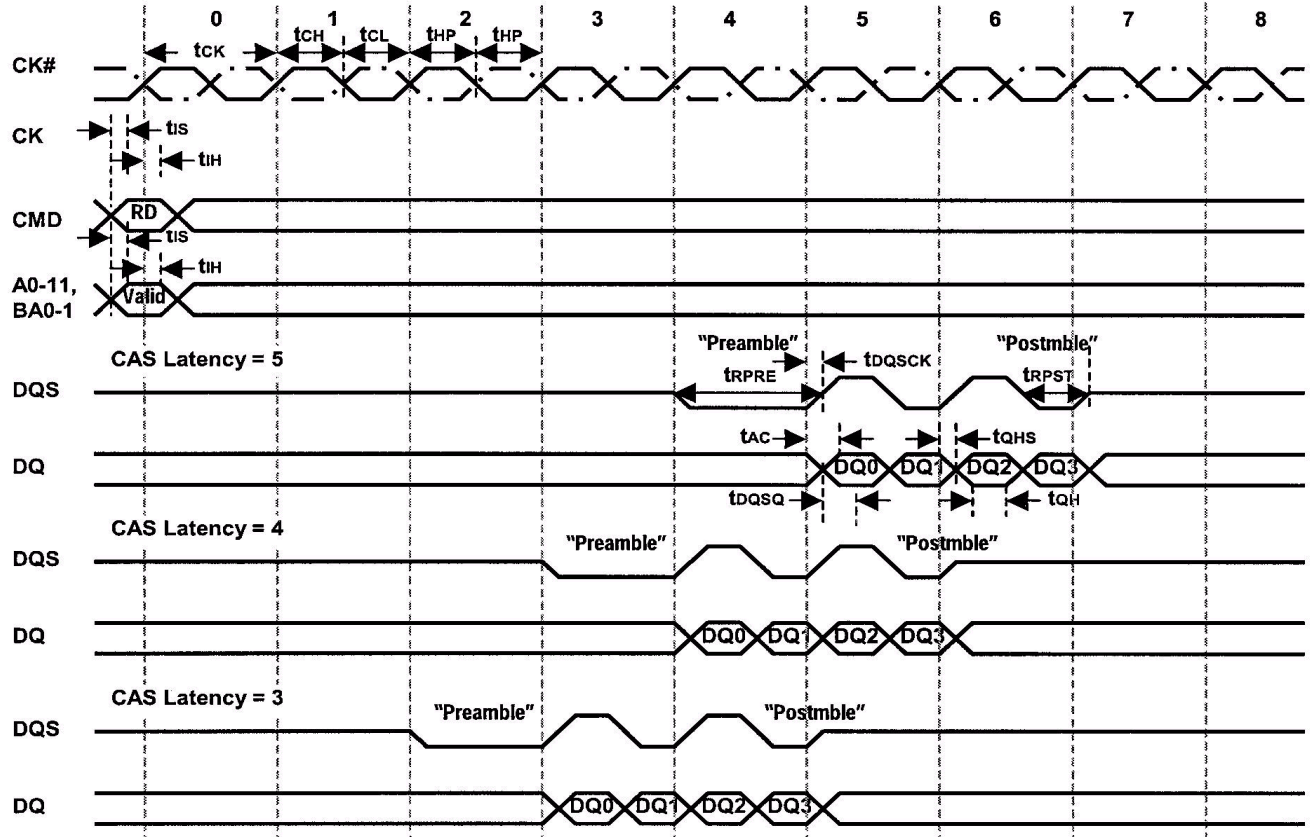


Figure 2. AC Parameters for Write Timing (Burst Length=4)

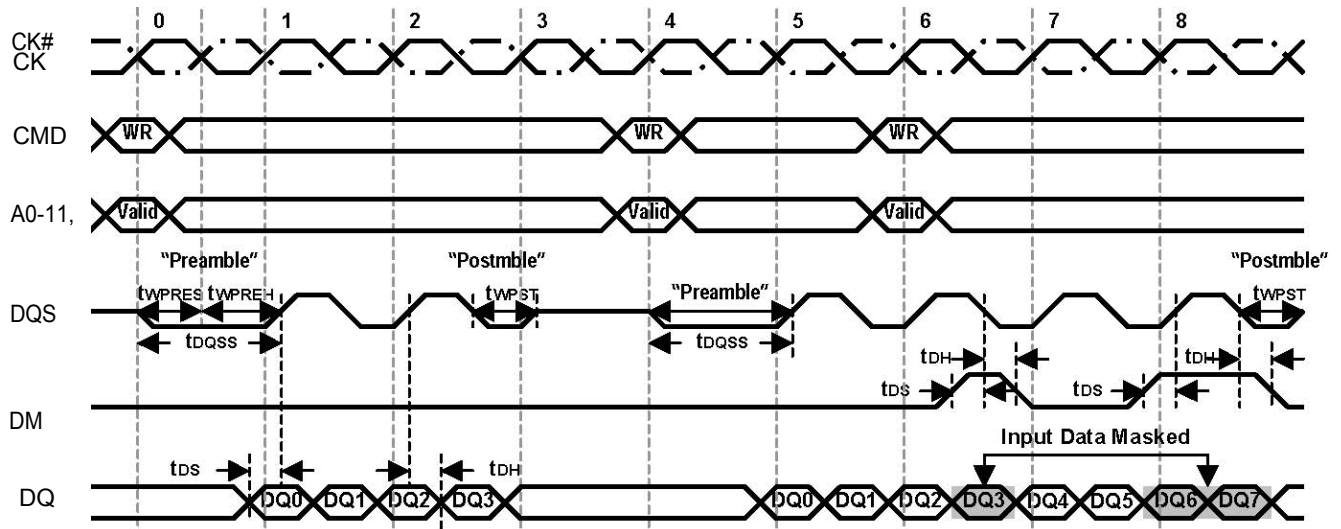


Figure 3. Bank Activate Read or Write Command Timing

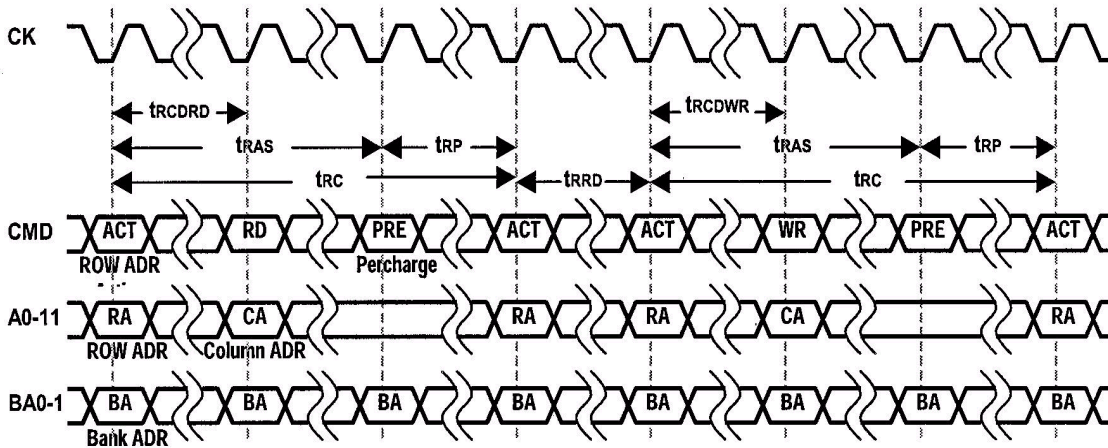


Figure 4. Burst Stop for Read (CAS Latency = 5, Burst Length = 4)

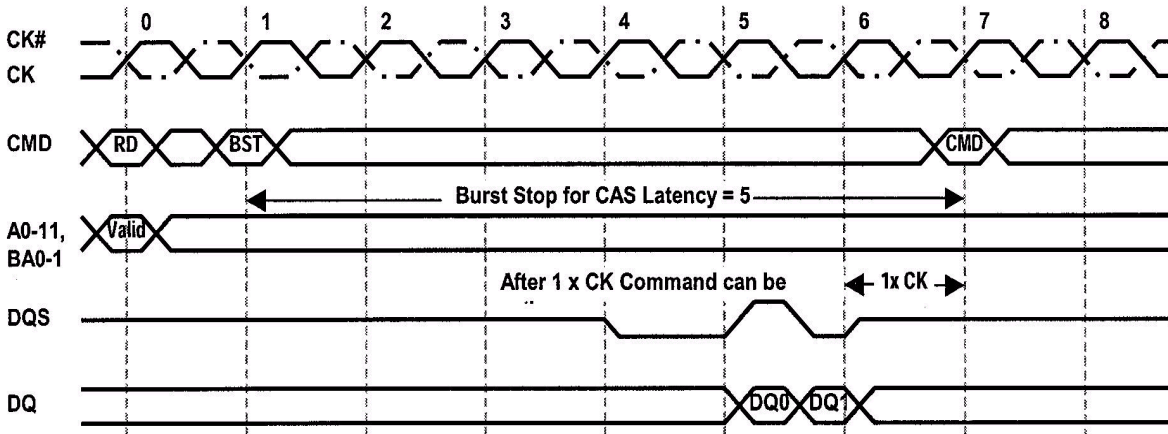


Figure 5. Read with Auto Precharge (CAS Latency = 5, Burst Length = 4)

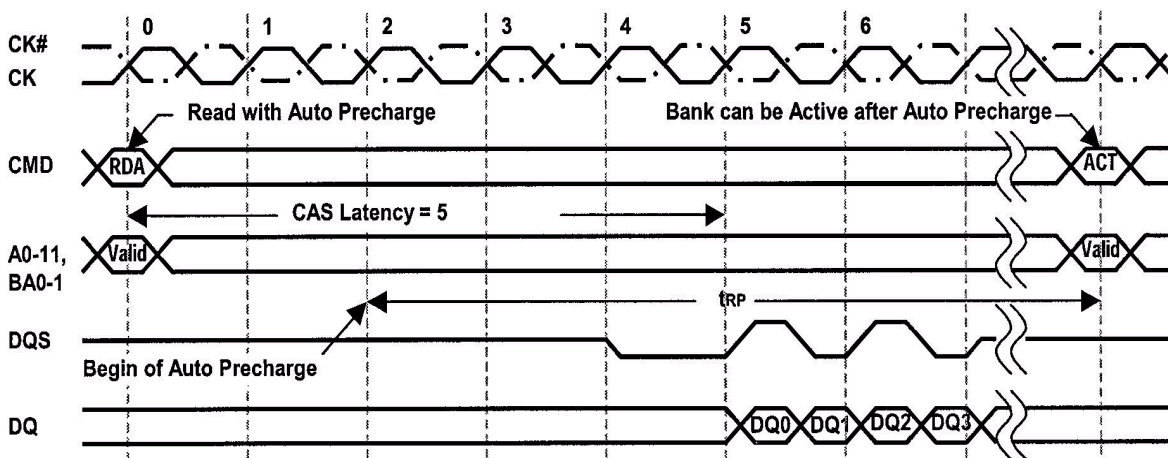


Figure 6. Write with Auto Precharge (Burst Length = 4)

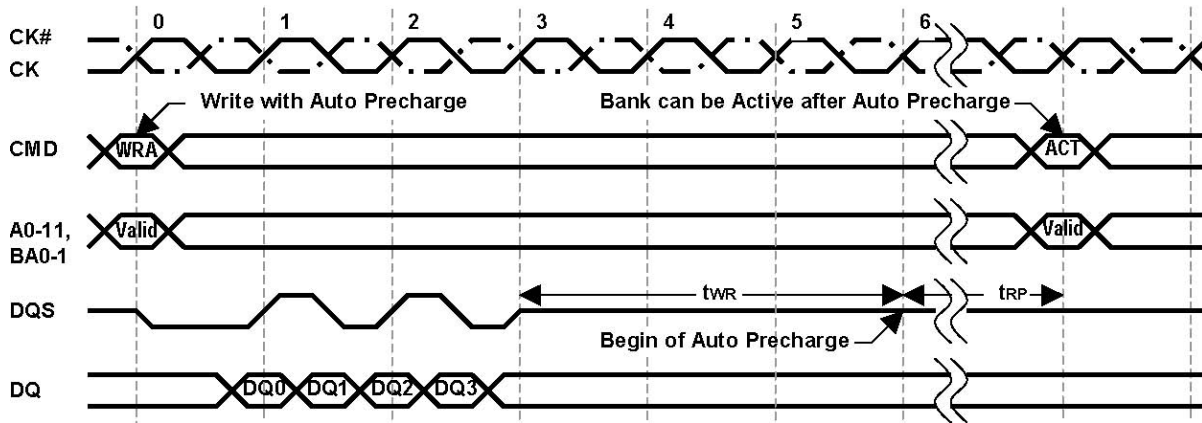


Figure 7. Read Burst Interrupt by Read (CAS Latency =5, Burst Length = 4)

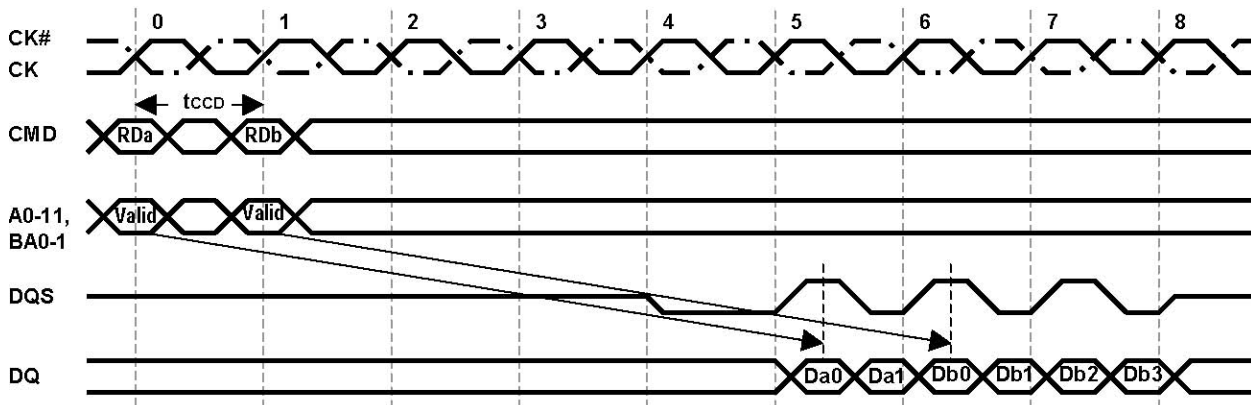


Figure 8. Write Interrupted by Write (Burst Length =4)

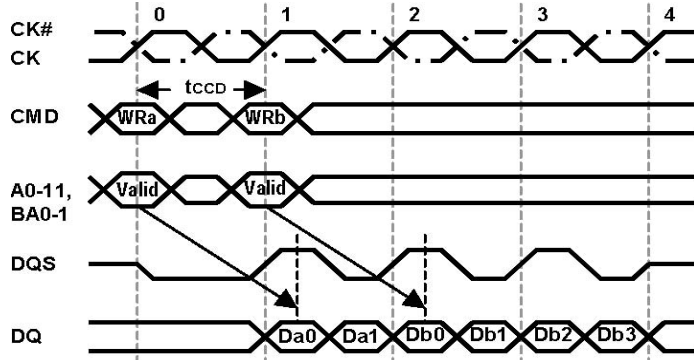


Figure 9. Auto Refresh Timing

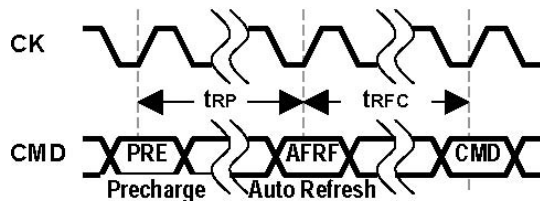


Figure 10. Self Refresh Timing

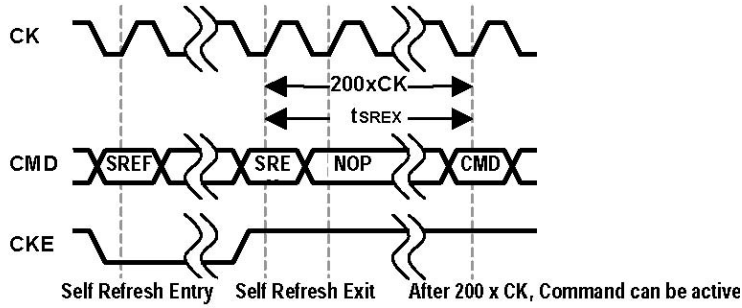


Figure 11. Precharge Command

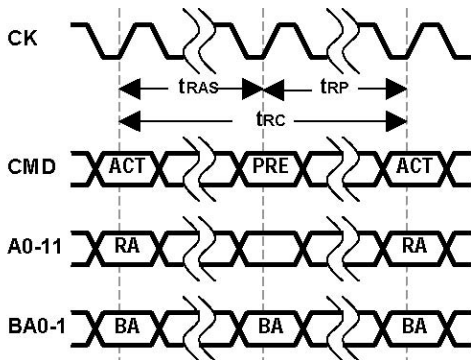


Figure 12. Power Up Sequence

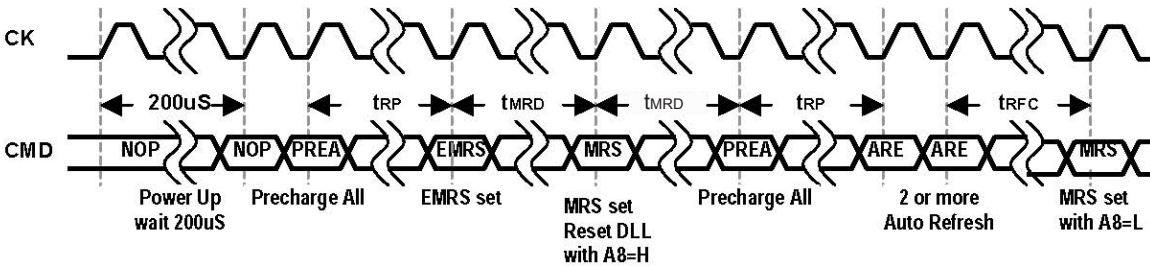


Figure 13. Mode Register Set Timing

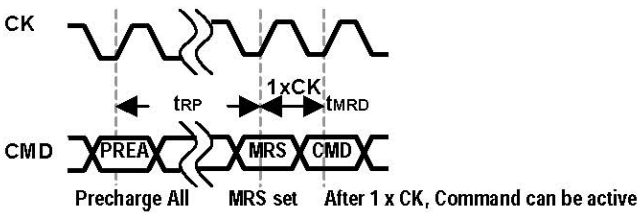
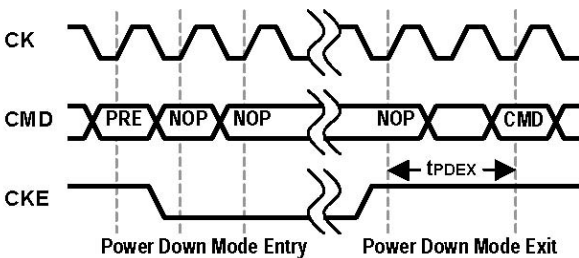
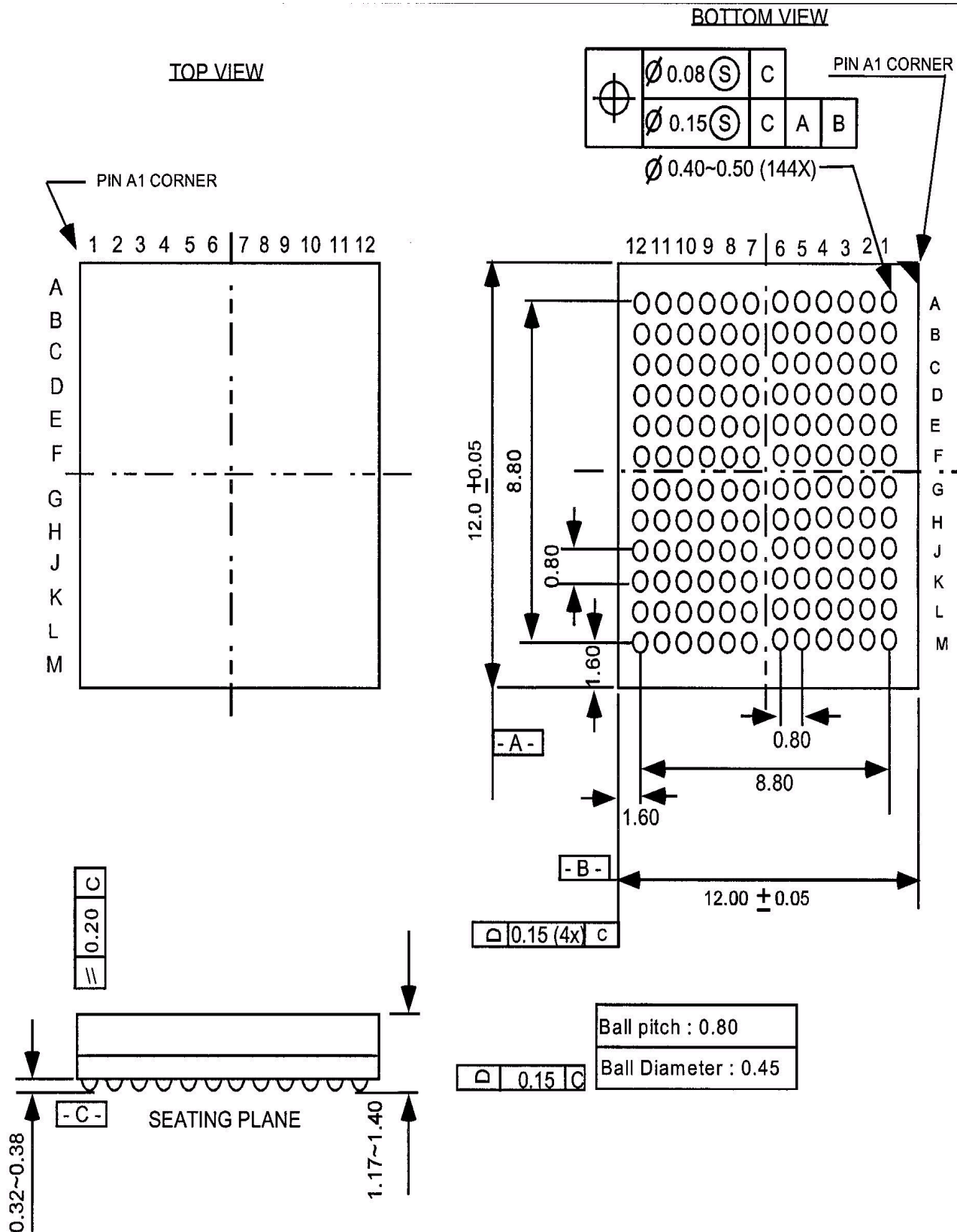


Figure 14. Power Down Mode





ORDERING INFORMATION (Pb-free Package)**Commercial Range: 0 °C to 70 °C**

Data rate	Speed (ns)	Order Part No.	Package
500MHz	4	IC43R32400-4B	144Ball FBGA
500MHz	4	IC43R32400-4BG	144Ball FBGA (pb-free)
400MHz	5	IC43R32400-5B	144Ball FBGA
400MHz	5	IC43R32400-5BG	144Ball FBGA (pb-free)

***Integrated Circuit Solution Inc.***

HEADQUARTER:
NO.2, TECHNOLOGY RD. V, SCIENCE-BASED INDUSTRIAL PARK,
HSIN-CHU, TAIWAN, R.O.C.

TEL: 886-3-5780333

Fax: 886-3-5783000

BRANCH OFFICE:
7F, NO. 106, SEC. 1, HSIN-TAI 5TH ROAD,
HSICHIH TAIPEI COUNTY, TAIWAN, R.O.C.

TEL: 886-2-26962140

FAX: 886-2-26962252

<http://www.icsi.com.tw>